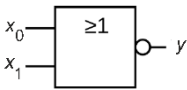


## NOR Gate

The **NOR gate (NOT-OR)** is a basic digital gate with multiple inputs and a single output. A HIGH output (1) results if both the inputs to the gate are LOW (0); if one or both input is HIGH (1), a LOW output (0) results. NOR is the result of the negation of the OR operator. It is a functionally complete operation. NOR gates can be combined to generate any other logical function. This property is called functional completeness<sup>1)</sup>.

The gate shown below has two inputs  $x_0$  and  $x_1$  but can be extended to any number of inputs.

IEC Symbol	Truthtable	Function															
	<table border="1"> <thead> <tr> <th><math>x_1</math></th><th><math>x_0</math></th><th><math>y</math></th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>0</td></tr> <tr> <td>1</td><td>0</td><td>0</td></tr> <tr> <td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	$x_1$	$x_0$	$y$	0	0	1	0	1	0	1	0	0	1	1	0	$\mathbb{B}^2 \rightarrow \mathbb{B}: y = \overline{x_1 + x_0}$ $\mathbb{B}^2 \rightarrow \mathbb{B}: y = \neg(x_1 \vee x_0)$
$x_1$	$x_0$	$y$															
0	0	1															
0	1	0															
1	0	0															
1	1	0															

Property	Settings	Meaning
<b>Inputs</b>	Standard	Number of inputs ( $x_0$ to $x_{n-1}$ )
<b>Data Bits</b>	Multi-Bit	Number of bits per input = Number of bits of output
<b>Delay</b>	Delays	Propagation delay from each $x_i$ to $y$ , $t_{pd} = t_{plh} = t_{phl}$
<b>Rejection Limit</b>	Delays	Inertial delay for all inputs $x_i$ All signal spikes shorter than the rejection limit are canceled. This is called pulse rejection: $t_{pd} \geq t_{inertial}$

<sup>1)</sup> <https://en.wikipedia.org>