

Tristate Gate

A **three-state**, **tri-state**, or **3-state** gate allows an output port to assume a high impedance state ('Z'), effectively removing the output from the circuit.

This allows multiple circuits to share the same output line or lines (such as a bus which cannot listen to more than one device at a time).¹⁾

Symbol	Truthtable															
	<table><tr><th><i>en</i></th><th><i>in</i></th><th><i>out</i></th></tr><tr><td>0</td><td>0</td><td>Z</td></tr><tr><td>0</td><td>1</td><td>Z</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table>	<i>en</i>	<i>in</i>	<i>out</i>	0	0	Z	0	1	Z	1	0	0	1	1	1
<i>en</i>	<i>in</i>	<i>out</i>														
0	0	Z														
0	1	Z														
1	0	0														
1	1	1														

Property	Settings	Meaning
Inputs	std_ulogic	Number of inputs (x_0 to x_{n-1})
Data Bits	multi-Bit	Number of bits per input = Number of bits of output
Delay	delay	Propagation delay from each x_i to y , $t_{pd} = t_{plh} = t_{phl}$
Rejection Limit	inertial delay	Inertial delay for all inputs x_i All signal spikes shorter than the rejection limit are canceled. This is called pulse rejection: $t_{pd} \geq t_{inertial}$

¹⁾ <https://en.wikipedia.org>
